AMENDMENTS TO THE SPECIFICATION:

Please amend the specification as follows:

Page 7, paragraph 2:

FIGS. 6A and 6B are diagrams showing signal processes performed by the input circuit 1, according to the first embodiment. The address signal A2 is initially supplied with the data-write command to the input circuit 1 as shown in FIG. 6A. The address signal A2 is one of the address signals A0 through A3 expressed by a combination of the least two significant bits (Y1, Y0) of an address. The address signal A2 supplied with the data-write command indicates that the input data is supplied to the input circuit 1 in order of the input data A2, A3, A0 and A1 after the address signal A2 is supplied thereto. If the address signal [[A4]] A3 is supplied with the data-write command to the input circuit 1, the input data is supplied to the input circuit 1 in order of the input data [[A4]] A3, A0, A1 and A2 after the address signal [[A4]] A3is supplied thereto. The input-point selector 12 selects the column N1 as a data input point of the shift register 14 by following the supplied address signal A2 as shown in FIG. 6A. Subsequently, the input data is supplied to the shift register 14 through the input buffer 10 by following a frequency of an internal clock CLK1 in the order of the input data A2, A3, A0 and A1. Since the input-point selector 12 selects the column N1 of the shift register 14 as the data input point, the input data supplied from the input buffer 10 is inputted to the column N1 continuously in the order of the input data A2, A3, A0 and A1. As a result, the columns N1, N0, N3' and N2' store respectively the input data A1, A0, A3 and A2 as

shown in FIG. 6B. The columns N1', N2 and N3 not storing the input data store a predetermined value, for example, a high-level signal or value as shown in FIG. 6B.